

## P1FE90VX3

### Power MOSFETs

900V, 1A, N-channel

#### Feature

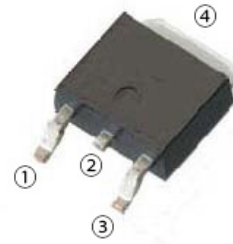
- N-channel
- SMD
- High Voltage (900V)
- Low Capacitance
- High Avalanche Durability, High di/dt Durability
- Based on AEC-Q101
- Pb free terminal
- RoHS:Yes

#### OUTLINE

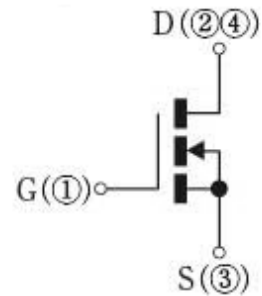
Package (House Name): FE

Package (JEDEC Code): TO-252AB similar

Package (JEITA Code): SC-63



#### Equivalent circuit



**Absolute Maximum Ratings** (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 150	°C
Channel temperature	Tch		-55 to 150	°C
Drain-source voltage	V <sub>DSS</sub>		900	V
Gate-source voltage	V <sub>GSS</sub>		±30	V
Continuous drain current(DC)	I <sub>D</sub>		1	A
Continuous drain current(Peak)	I <sub>DP</sub>	Pulse width 10μs, duty=1/100	4	A
Continuous source current(DC)	I <sub>S</sub>		1	A
Total power dissipation	P <sub>T</sub>		36	W
Repetitive avalanche current	I <sub>AR</sub>	Starting Tch=25°C Tch≤150°C	1	A
Single avalanche energy	E <sub>AS</sub>	Starting Tch=25°C Tch≤150°C	10	mJ
Repetitive avalanche energy	E <sub>AR</sub>	Starting Tch=25°C Tch≤150°C	1	mJ
Drain - source diode di/dt strength	di/dt	I <sub>s</sub> =1A, Tc=25°C	350	A/μs

※ :See the original Specifications

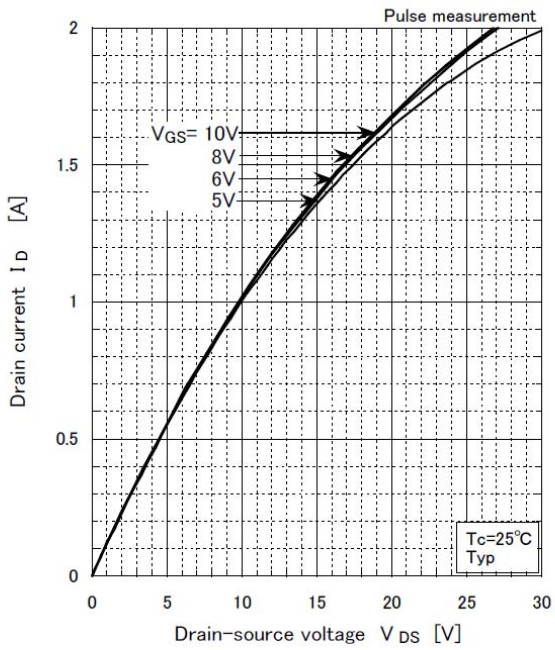
**Electrical Characteristics** (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	900			V
Zero gate voltage drain current	$I_{DSS}$	VDS=900V, VGS=0V			100	μA
Gate-source leakage current	$I_{GSS}$	VGS=±25V, VDS=0V			±10	μA
Forward transconductance	$g_{fs}$	ID=0.5A, VDS=10V	0.7	1.5		S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=0.5A, VGS=10V		9.5	14	Ω
Gate threshold voltage	$V_{th}$	ID=0.2mA, VDS=10V	3	3.5	4	V
Source-drain diode forward voltage	$V_{SD}$	IS=0.5A, VGS=0V			1.5	V
Thermal resistance	$R_{th(j-c)}$	Junction to case, with heatsink			3.4	°C/W
Total gate charge	$Q_g$	VDD=400V, VGS=10V, ID=1A		10.8		nC
Input capacitance	$C_{iss}$	VDS=25V, VGS=0V, f=1MHz		193		pF
Reverse transfer capacitance	$C_{rss}$	VDS=25V, VGS=0V, f=1MHz		5.2		pF
Output capacitance	$C_{oss}$	VDS=25V, VGS=0V, f=1MHz		27.3		pF
Turn-on delay time	$t_{d(on)}$	ID=0.5A, RL=300Ω, VDD=150V, Rg=50Ω, VGS(+)=10V, VGS(-)=0V		8.4		ns
Rise time	$t_r$	ID=0.5A, RL=300Ω, VDD=150V, Rg=50Ω, VGS(+)=10V, VGS(-)=0V		15		ns
Turn-off delay time	$t_{d(off)}$	ID=0.5A, RL=300Ω, VDD=150V, Rg=50Ω, VGS(+)=10V, VGS(-)=0V		40		ns
Fall time	$t_f$	ID=0.5A, RL=300Ω, VDD=150V, Rg=50Ω, VGS(+)=10V, VGS(-)=0V		24		ns

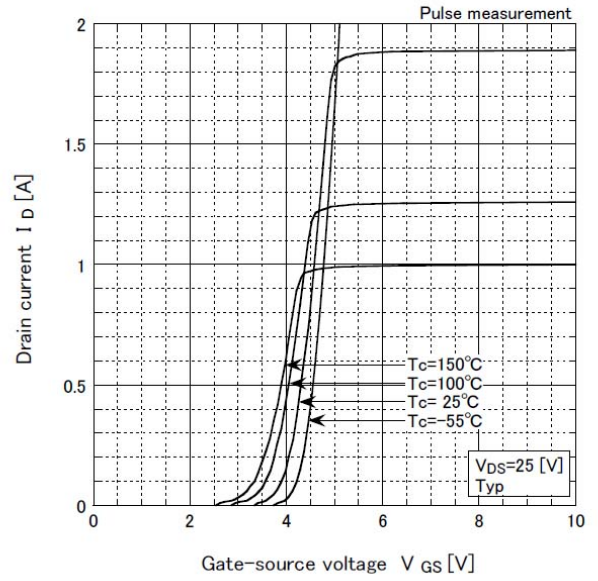
※ : See the original Specifications

# CHARACTERISTIC DIAGRAMS

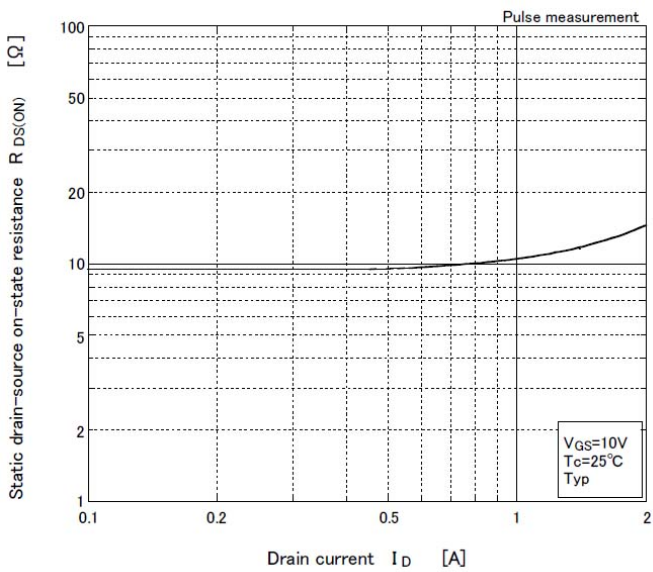
Typical output characteristics



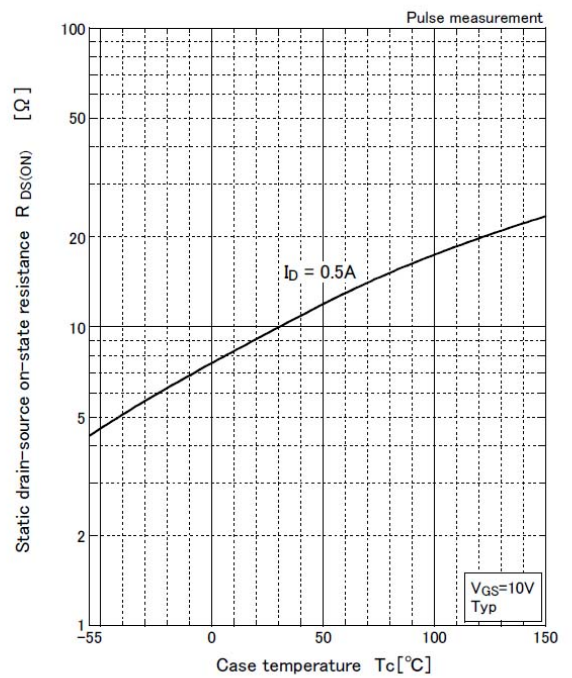
Transfer characteristics



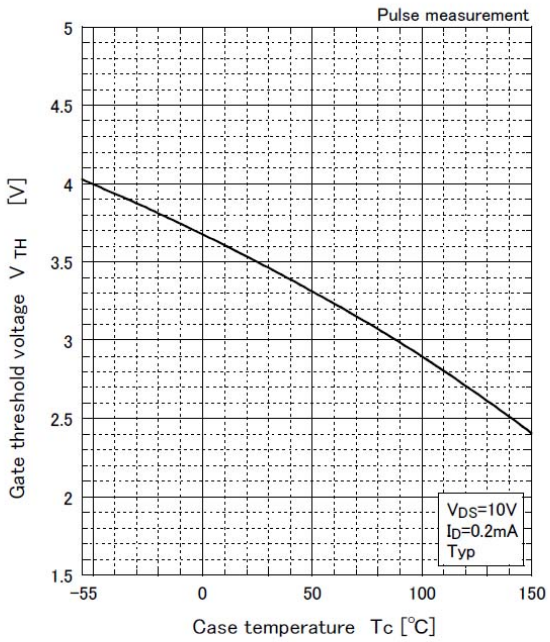
Static drain-source on-state resistance vs drain current



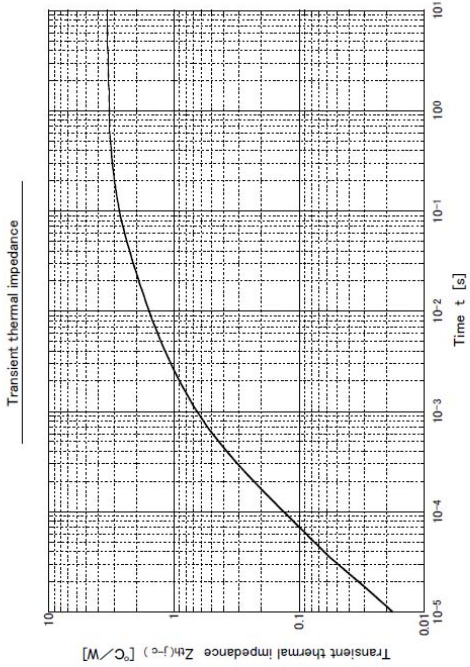
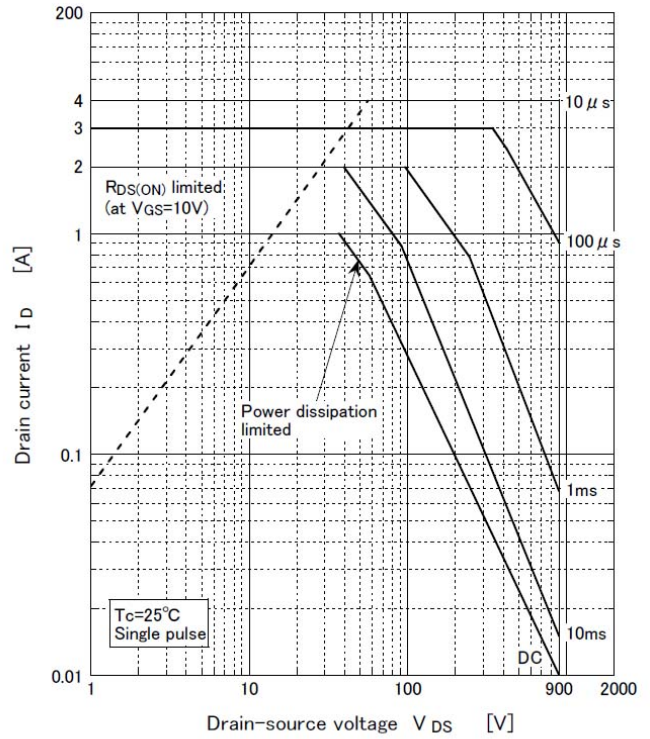
Static drain-source on-state resistance vs case temperature



Gate threshold voltage vs case temperature

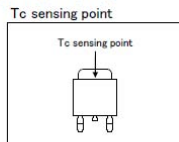


Safe operating area

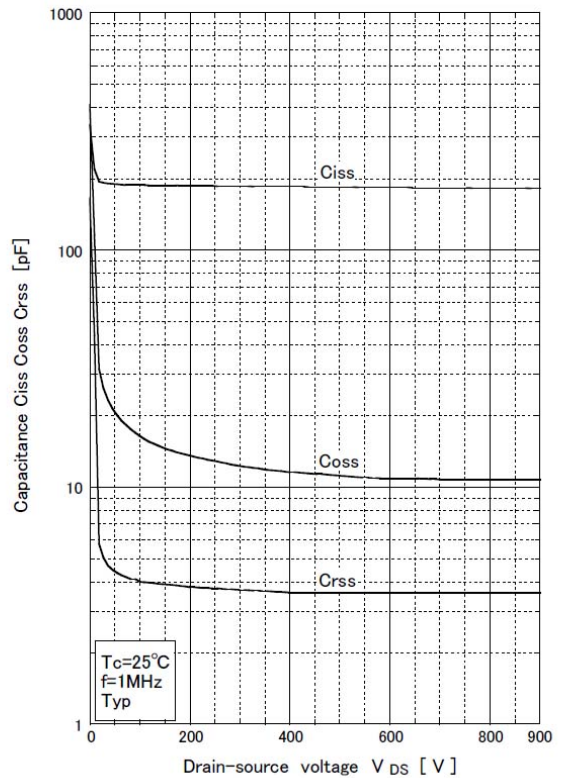


Substrate detail

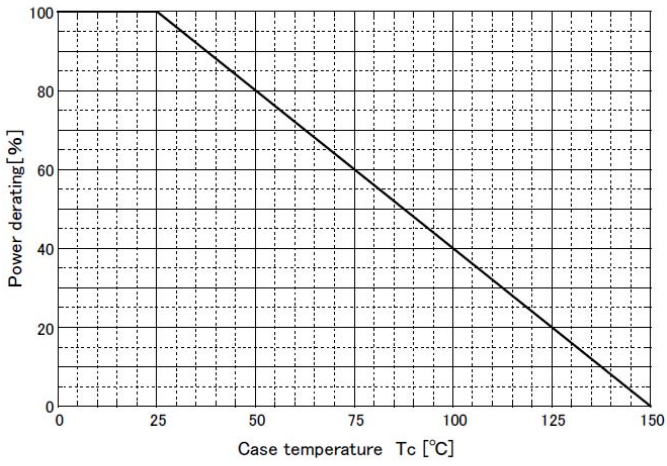
Type	Alumina
Size	1 inch <sup>2</sup>
Thickness	0.64mm
Conductor thickness	20 $\mu m$
Pattern area	65mm <sup>2</sup>



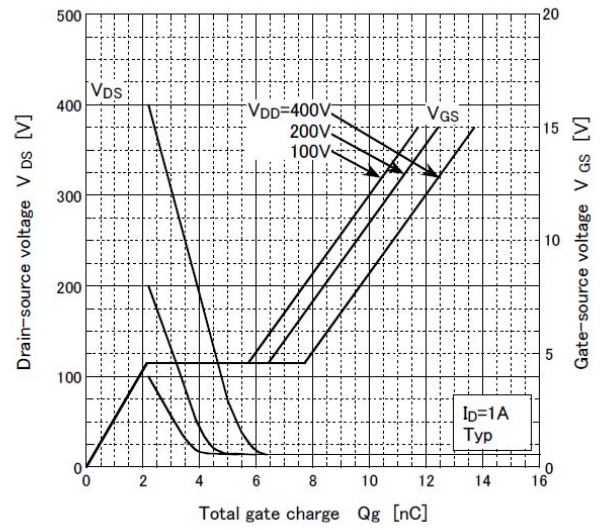
Capacitance characteristics



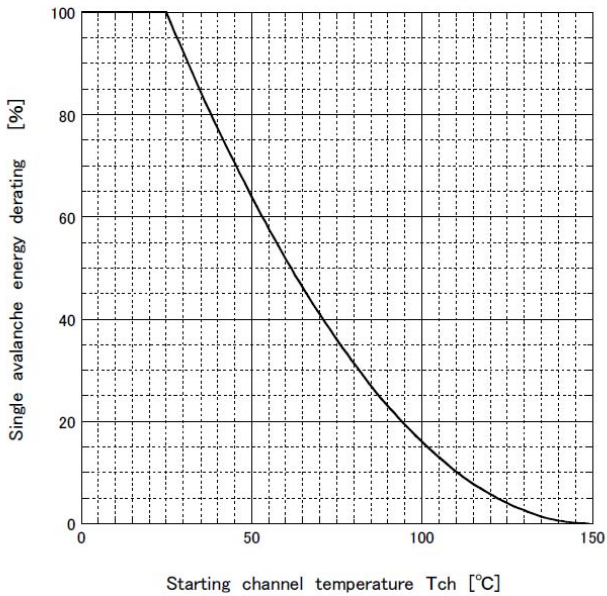
Power derating - case temperature



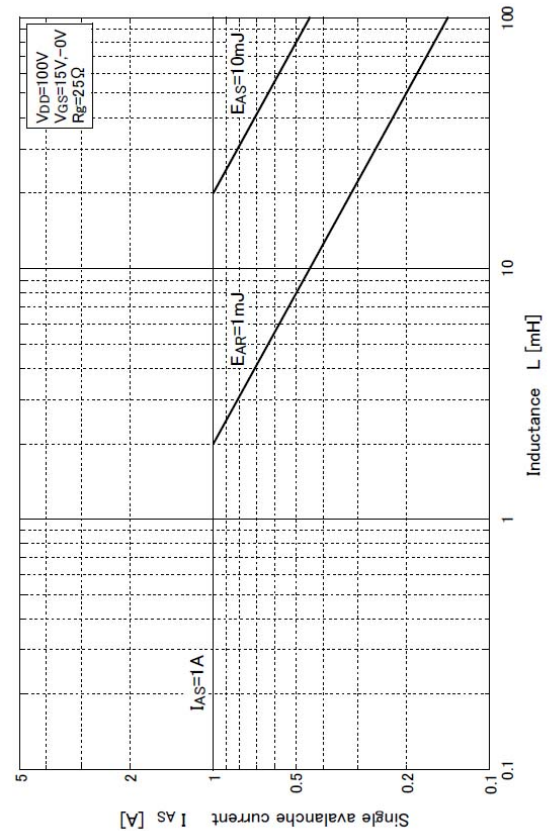
Gate charge characteristics



Single avalanche energy derating vs channel temperature

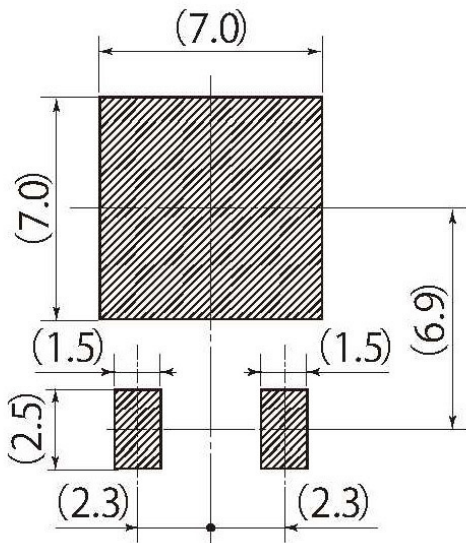
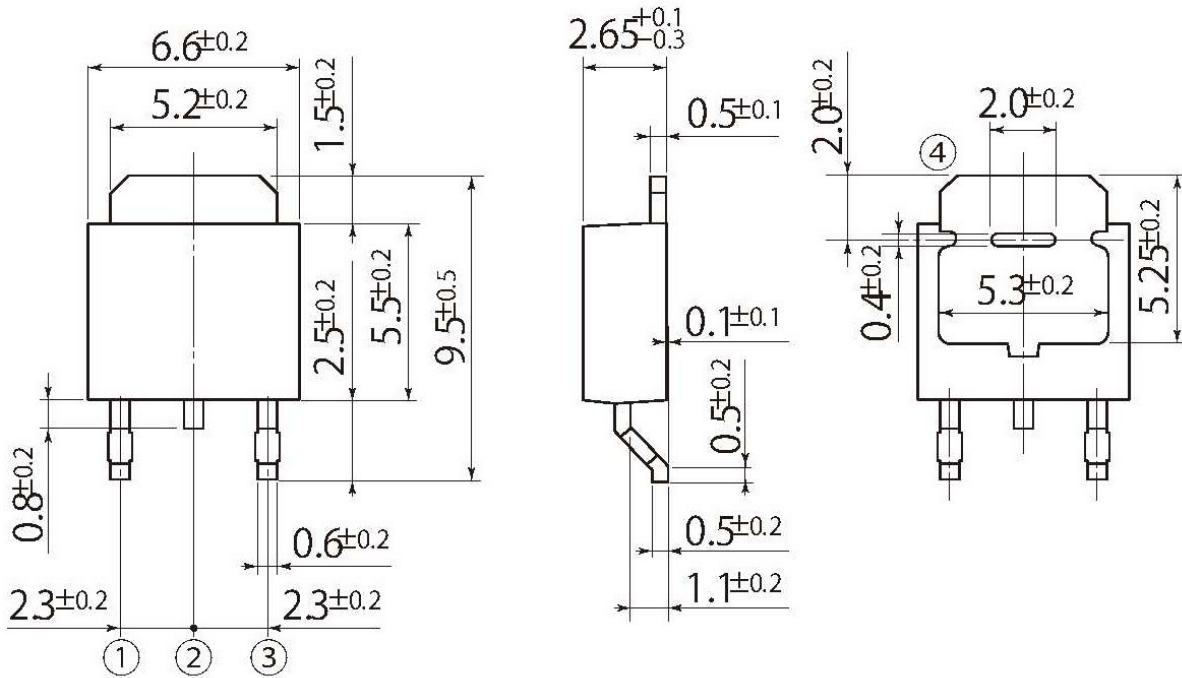


Single avalanche current vs inductive load



G3

JEDEC Code	TO-252AB similar
JEITA Code	SC-63
House Name	FE



Referential Soldering Pad

• Optimize soldering pad to the board design and soldering condition.

## Notes

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